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Leakage Current Reduction Techniques for CMOS Circuits

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Abstract

Most of the portable systems, such as cellular communication devices, and laptop computers operate from a limited power supply. Devices like cell phones have long idle times and operate in standby mode when not in use. Consequently, the extension of battery- based operation time is a significant design goal which can be made possible by controlling the leakage current flowing through the CMOS gate. Leakage Current loss is a major concern in nanometer and deep submicron technologies. In this paper we use different techniques to reduce leakage power. Based on the surveyed techniques a designer is able to select appropriate leakage current reduction technique.

Keywords: Dual Vth, Transistor Stack, Sleep Transistor, Forced Transistor Stack, MTCMOS, VTCMOS, SCCMOS, , LECTOR, GALEOR

Introduction

Low power consumption in high performance VLSI circuits is highly desirable aspect as it directly relates to battery life, reliability, packaging, and heat removal costs. With the continuous trend of technology scaling, leakage power is becoming major contributor to the total power consumption in CMOS circuits. Scaling of Vdd reduces dynamic power consumption but degrades the performance of the circuit as well. This can be partially compensated by lowering Vth but at cost of increased leakage power. Minimizing leakage power consumption is currently an extremely challenging area of research, especially with on-chip devices doubling every two years. Leakage power dissipation arise from the leakage currents flowing through the transistor when there are no input transitions and the transistor has reached steady state. Unlike dynamic power, leakage power depends on the total number of transistors in the circuits, their types, and their operation status regardless of their switching activity.

The remaining part of this paper is organized as follows. Section 2 describes Leakage current mechanisms in standby mode. Section 3 surveys on leakage current reduction techniques Section 4 concludes this paper.

Leakage Current Mechanisms in Standby

Generally, Power dissipation consists of dynamic and static power dissipation. Dynamic power dissipation is due to the unnecessary switching activity in the transistors .Components of static power dissipation are Reverse biased junction leakage (I_1), Sub-threshold leakage (I_2), oxide tunneling current (I_3), gate current due to hot carrier injection (I_4), gate induced drain leakage (I_5), punch through leakage (I_6). Currents I_2, I_5 and I_6 are off-state leakage mechanisms, while I_1 and I_3 occur in both ON and OFF states. I_4 can occur in the off state, but more typically occurs during the transistor bias states in transistion[5].

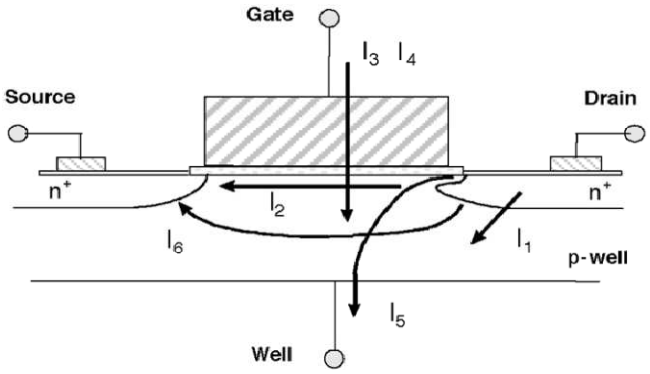

Fig 1. Summary of leakage mechanisms of NMOS Transistor[5]

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Reverse biased junction leakage (I_{REV}) is due to the small reverse bias leakage current flowing between the source/drain and substrate regions. Sub-threshold leakage (I_{SUB}) is due to current flow between source and drain regions when the transistor is biased in cut-off. Gate oxide tunneling current is due to the tunneling of electrons between the gate and substrate regions when high electric fields are applied across the gate oxide region. Hot carrier injection results due to the lowering of threshold voltage by electrons/holes. Gate induced drain leakage (I_{GIDL}) will results due to the movement of minority carriers between channel and substrate regions due to the application of large negative gate bias. Punch through leakage is due to the current flowing between source and drain regions when channel disappears.

Leakage Current Reduction Techniques

Leakage is becoming comparable to dynamic switching power with the continuos scaling down of CMOS technology. To reduce leakage current, many techniques have been proposed, including dual-V_{th} CMOS, Transistor Stacking, Sleep Transistor, Forced Transistor Stack, MTCMOS,VTCMOS, SCCMOS, LECTOR, GALEOR.

Dual V_{th} CMOS

Dual V_{th} CMOS is an efficient technique for leakage reduction. In this method, each cell in the standard cell library has two versions, low V_{th} and high $V_{th..}$ For a logic circuit, a higher threshold voltage can be assigned to some transistors in non-critical paths so as to reduce the leakage current, while the performance is maintained due to the use of low threshold transistors in the critical paths. Therefore, no additional leakage control transistors are required, and both high performance and low power can be achieved simultaneously.

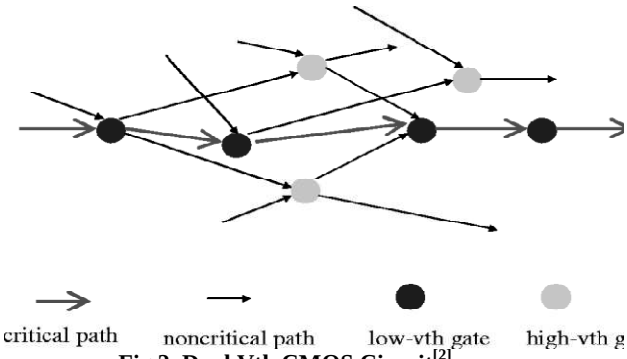

Fig 2. Dual Vth CMOS Circuit[2].

Fig 2 illustrates the basic idea of a dual V_{th} circuit. Dual threshold technique is good for leakage power reduction during both standby and active modes without delay and area overhead.

Transistor Stacking

The two serially connected devices in the off state have significantly lower leakage current than a single off device. This is called the stacking effect[10]. With transistor stacking by replacing one single off transistor with a stack of serially connected off transistors, leakage can be significantly reduced. The disadvantages of this technique are performance degradation or more dynamic power consumption.

Sleep Transistor Technique

This is a technique in which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is similar to MTCMOS, which adds high V_{th} sleep transistors between pull-up networks and V_{dd} and pull-down networks and gnd while for fast switching speeds, low V_{th} transistors are used in logic circuits [6]. This technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep.

Forced Transistor Stack

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turned off. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time.

Multi Threshold Voltage CMOS (MTCMOS)

A Multi Threshold Voltage CMOS (MTCMOS) reduces the leakage by inserting high threshold devices in series to low V_{th} circuitry. Fig 3(a) shows the schematic of an MTCMOS circuit. A sleep control scheme is introduced for efficient power management. In the active mode, SL is set low and sleep control high V_{th} transistors (MP and MN) are turned on. Since their on-resistances are small, the virtual supply voltages (VDDS and VSSV) almost function as real lines. In the standby mode, SL is set

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high, MN and MP are turned off, and the leakage current is low.

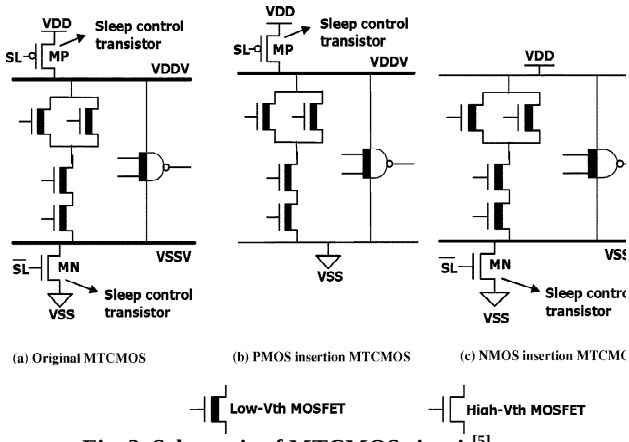

Fig. 3. Schematic of MTCMOS circuit[5].

In fact, only one type of high Vth transistor is enough for leakage control. Fig. 3(b) and (c) shows the PMOS insertion and NMOS insertion schemes, respectively. The NMOS insertion scheme is preferable, since the NMOS on-resistance is smaller at the same width; therefore, it can be sized smaller than corresponding PMOS. However, MTCMOS can only reduce the standby leakage power, and the large inserted MOSFETs can increase the area and delay.

Super Cutoff CMOS Technique (SCCMOS)

This technique has been proposed to solve the problem of the extra cost of the MT approach. The basic idea behind this method is to turn off completely the transistor which connects the main circuit to V_{DD} or GND. This is achieved by connecting the gate of the transistor to a voltage which is higher than V_{DD}. This leads to a positive V_{gs} for a PMOS transistor (fig 4) and, hence the sub threshold current reduces exponentially with increasing this voltage.

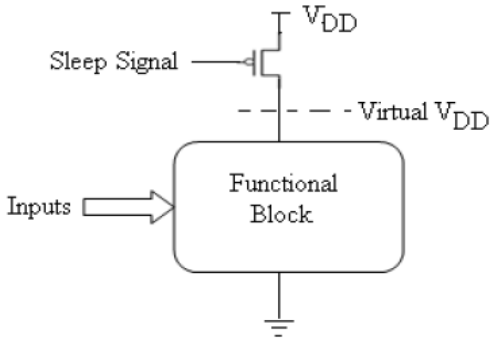

Fig. 4. SCCMOS Concept[4]

Variable Threshold CMOS (VTCMOS)

Variable Threshold CMOS (VTCMOS) is a circuit design technique that has been developed to reduce standby leakage currents in low VDD and low VT applications[2]. VTCMOS circuit uses low threshold voltage transistors, and the substrate bias voltages of the NMOS and PMOS transistors are generated by the variable substrate bias control circuit. The disadvantage of the VTCMOS is it requires separate power pin if the substrate bias voltage levels are not generated on chip.

LECTOR Technique

As its name implies, Leakage Control TransistOR technique (LECTOR) introduces LCT in each CMOS gate as shown in fig 5. Since one of the LCTs is always near its cut off, it causes increase in resistance in the path from VDD to ground leading to decrease in leakage current[1].

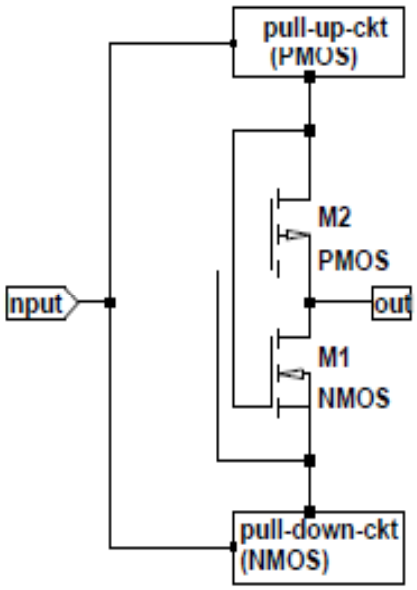

Fig. 5. LECTOR Technique[1]

The basic approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This states that " A state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path". The LECTOR implementation involves the addition of two LCTS for each gate between the supply and ground path.

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GALEOR Technique

As its name implies, **GA**ted **LE**akage Transist**OR** technique (GALEOR) introduces GLT in each CMOS gate as shown in Fig 6. In this technique the maximum reduction in leakage power is achieved by introducing high threshold voltage transistors, thereby increasing circuit delay[3]. It reduces the leakage current flowing through the circuit. In this technique two gated leakage transistors are inserted between NMOS and PMOS circuitry of the existing circuit such that gates of the extra inserted transistors are connected to their respective drain regions. This technique reduces the output voltage swing due to the threshold voltage loss caused by the addition MOS transistors. Reduced voltage swing increases the propagation delay through the circuit.

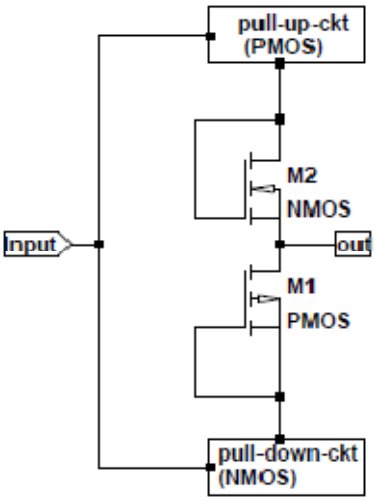

Fig. 6. GALEOR Technique[1]

Conclusions

As technology scales down to the nanometer technologies , the leakage current becomes more critical in portable systems where battery life is of prime concern. Based on the surveyed techniques, a designer would be able to select the appropriate leakage optimization technique for a particular level of an application.

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